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A Scalable ATM Switching System Architecture

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Abstract—**The architecture of an ATM switching system for prototype applications is presented. After introducing the general concept to upgrade the existing ISDN switch with an ATM module, the building blocks of this ATM module are described in more detail. Switching of ATM cells is performed in a single ASIC, which can be cascaded forming large switching modules. Peripheral modules interface the ATM switch to external transmission systems and perform all ATM-related functions, including means for redundancy of the switching network. The redundancy scheme explained in the paper tolerates single failures without affecting the user information. Finally, a switching network architecture is shown to be capable of fulfilling the varying demands in terms of the number of ports for ATM switches and cross connects, concentrators, and multiplexers. It is the basis for the implementation of systems which range from very small to very large (several thousand ports), and which can be upgraded over the entire range without service interruption.**

I. Introduction

FOR future applications which require bit rates of significantly more than 64 kb/s, which is the standard bit rate in the existing and still evolving narrowband networks, the *asynchronous transfer mode* (ATM) is internationally agreed upon as the target multiplexing and switching principle, at least for interactive services. Thus, ATM has become the basis of a future broadband ISDN (B-ISDN).

The main objectives which had to be reached by the definition of this target principle have been:

- *Flexibility with respect to bit rates.* For the large variety of bit rate requirements of future services, the currently small set of fixed discrete bit rate values of the standard transmission systems is not appropriate.
- *Asymmetrical connections.* Several applications (e.g., data base browsing, retrieval of graphics etc.) require a high bit rate only in one direction.
- *Capability of supporting services with variable bit rates* (e.g., video services).
- *Universal multiplexing and switching principle.* All possible services should be supported by a single network in order to avoid a large number of small, service-specific networks which are undesirable from an economic point of view.
- *Support of multimedia-applications.* Multiple connections (e.g., data, graphics, voice annotation, video) with different service requirements can be handled within a single call, only in a homogeneous network.

In the introduction phase of broadband networks, only a limited number of customers will be connected to the ATM switching nodes. For the network operating companies, it is essential, therefore, to keep the initial investment for the switching systems as low as possible and to be able to enhance these systems over a wide range in terms of the numbers of ports when required. Estimates of growth of the networks and systems, which would facilitate their planning, are very difficult for several reasons.

- Characteristics of new services are not fully known. For the time being, some services might not even be known at all. Other services, like video conferencing and other video services, are still changing their bit rate requirements in connection with advances in coding theory and technology.
- Growth of new services, in general, is difficult to predict correctly.

In order to deal with such a high degree of uncertainty, architectures for ATM switching systems have to be scalable from very small to very large (thousands of ports) and have to be extendible over an equally wide range.

The paper is organized as follows: In Section II, a scalable system architecture is presented which is currently under development as a prototype system. Section II-A contains the overall system architecture of a B-ISDN switching system based on the EWSD narrowband switching system. The structure of the ATM part is discussed in detail in Section II-B. Section II-C presents the generic system building blocks of the ATM switch: the ATM switching element, the ATM switching module, and the interface modules. Section II-D presents the redundancy concept, which guarantees a high availability of the ATM switching system kernel. Finally, the switching network is discussed in detail in Section II-E. Special emphasis is placed on the properties which are crucial for the scalability of the system. Section III then gives some outlook on further development steps of the Siemens ATM system.

II. System Architecture

A. Overall System Structure

It is accepted worldwide that the asynchronous transfer mode (ATM) is the basic multiplexing and switching principle for wideband and broadband services. For nar-

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rowband services, a circuit switched network is currently evolving which will serve a large installed customer base at the time of introduction of an ATM-network.

Therefore, the SIEMENS pilot ATM switch has been designed as an enhancement to the existing and still evolving EWSD narrowband switching system. The system consisting of EWSD along with its ATM module will then be called EWSD-B to reflect its broadband switching capability [1].

A detailed description of EWSD is beyond the scope of this paper. Though, a short outline of its main functional blocks is pertinent in order to understand the way of interworking between both parts of EWSD-B.

As shown by Fig. 1, the narrowband part consists of the:

- *Digital line unit* (DLU) for the accommodation of subscriber lines (analog and digital). The interface to the switching system kernel is formed by DS1 transmission systems.
- *Line trunk group type C* (LTGC) for the connection of DLU's and trunks. Each LTGC contains a *group processor* (GP), which is responsible for call processing, maintenance, and safeguarding aspects related to subscriber lines and trunks.
- *Circuit switching network* (CSN), which carries user and control information (switched or semipermanent) based on $n \times 64$ kb/s channels.
- *Coordination processor* (CP) for central database management, switching control, safeguarding, operation, administration, and maintenance.
- *Common channel network control* (CCNC) for the handling of the message transfer part of the common channel signaling system no. 7.

In a similar way, the broadband part consists of the:

- *Line trunk group type E* (LTGE) for broadband connections which accommodates ATM subscriber lines, ATM trunks, and DS1 transmission systems. The interface to the switching network is formed by a number of ATM-oriented links with a proprietary ATM protocol (more about this interface can be found in the following section of the paper). Each LTGE contains a *group processor* (GP) which basically handles the same functions as the GP in the narrowband part.
- *ATM switching network* (ASN), which carries user and control information (switched or semipermanent) based on virtual connections.
- *Remote unit* (RU) as remote multiplexer concentrator for broadband subscriber lines.

The coupling between the ATM and the narrowband parts is achieved by DS1 transmission systems for user information between LTGC and LTGE, and an additional ATM-oriented interface to the CP for control information.

B. ATM System Structure

1) Hardware Structure: The ATM system has been designed according to the following basic principles.

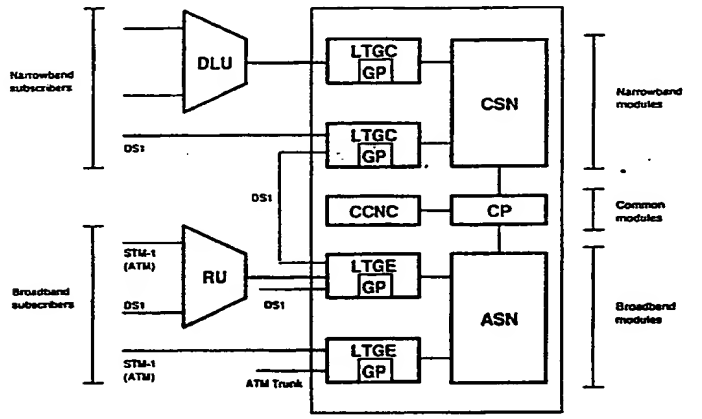

Fig. 1. EWSD-B system architecture.

- The system has to be well suited for broadband service switches as well as cross-connect systems with the possibility to perform both functions in the same switching network.
- The switching network employs the self-routing principle.
- All connection-related information which is needed during an active call is stored only in those peripheral units (e.g., line modules, trunk interfaces, · · ·) which are affected by the particular connections. This means that the large translation tables which have to accommodate the per-connection information for several thousands of simultaneous virtual connections and/or virtual paths are held only in one location in the system for quick access (of course, a backup of this information is also available in the processors).
- The ATM switching network should be testable in a simple way. This can be achieved by test cells which can be routed arbitrarily in order to check all possible paths.
- Only one internal user data interface definition is employed.

Fig. 2 shows the principal structure for the EWSD-B broadband part consisting of LTGE, RU, and ASN. The functional units and their tasks within the system are as follows.

- *Subscriber line module broadband* (SLMB) for the connection of broadband subscriber lines with SDH transmission interfaces, in a first step for STM-1 (155 Mb/s), and also later on for STM-4 (622 Mb/s) in a concatenated version (VC-4-4c).
- *Trunk interface unit* (TIU) for the connection of trunks and feeder lines to remote units with SDH transmission interfaces, in a first step for STM-1 (155 Mb/s, VC-4), and also later on for STM-4 (622 Mb/s, VC-4-4c).
- *Digital interface unit* (DIU) for DS1 systems performing as an interworking unit with existing narrowband exchanges or DS1 terminals. In further development steps, some other interworking units will also be available.
- *Group processor* (GP).
- *ATM multiplexer* (AMX) for the concentration of

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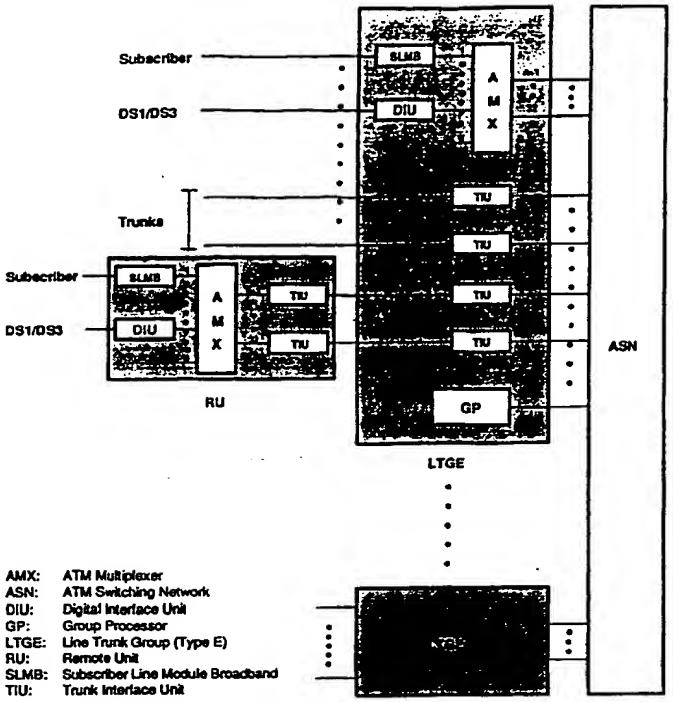

Fig. 2. EWSD-B ATM system structure.

subscriber traffic. The AMX uses the same switching module (32 × 32) as the ATM switching network (ASN), but configuration allows for concentration ratios between 1 : 1 and 31 : 1 depending on the traffic requirements.

All the units SLMB, TIU, DIU, and GP have the same type of interface to AMX and ASN, i.e., a proprietary ATM protocol which adds some additional information to the ATM cell as it is defined by CCITT [2]. This additional information requires an increase of the bit rate compared to the external SDH payload bit rate.

The additional information consists of routing tags defined at call setup for each individual virtual connection, which determine the path of each individual cell through all stages of the ASN, and some synchronization, housekeeping, control and test information for ASN internal purposes. This information is inserted into, respectively removed from each cell by the aforementioned peripheral units SLMB, TIU, DIU, GP. The routing information is derived from the routing field of the ATM cell (VCI/VPI). In the case of SLMB and TIU, an address translation from the incoming address to the outgoing address (in terms of VCI/VPI of the standard cell header) is performed. In the case of DIU and GP, the virtual connection (VC or VP) will be terminated.

As shown in Fig. 2, LTGE and RU consist of the same building blocks: SLMB, DIU, TIU, and AMX. An RU is connected to an LTGE by means of feeder lines which are terminated by TIU modules. In the case of a large RU, a GP can be added in order to allow for stand-alone operation, and the AMX can be replaced by a larger multistage (ASN-like) structure for the accommodation of a larger number of subscribers.

2) Control Structure: Although (in the hardware structure) a GP is associated with an LTGE, interface units can in fact be freely allocated to GP's, irrespective of their physical location since GP's as well as interface modules are all interconnected via the ATM switching network. Thus, the number of group processors can be adjusted to the requirements for call handling capacity. It is independent of the number of ports of being served, or their bit rate.

C. System Building Blocks

1) ATM Switching Element: The ATM switching element (SE) is the basic element of the ATM switching network and has been realized by a single CMOS chip with about 780 000 transistor functions. The functional structure of the switching element is shown in Fig. 3. It contains a central shared buffer with logical output queues and is controlled by the routing information in each internal cell header. This architecture has been found superior to other solutions. In terms of performance, the chosen switching element implementation is optimum due to the use of output queueing, which is known to yield the lowest possible queueing delays, and the shared buffer which minimizes the amount of memory required for the buffers [3]. Concentration of all complex functions in a single ASIC allows a system design based on good modularity, and leads to an equipment practice suitable for production and large-scale switches also. Reference [4] gives an overview to ATM switching principles; examples for ATM switches can be found, e.g., in [5]–[7].

The main function of the SE is to route arriving ATM cells from sixteen input lines to the desired output (of eight output lines) or to the module processor in the case of switch-internal message cells. These special cells are indicated by a flag in the internal routing header. Bit-phase alignment, priority handling, and self tests for logic and RAM areas are included on the 216 mm^2 silicon device. Fig. 4 shows the photography of the SE 16/8 chip. More details of this device are described in [8].

The regularly structured block in the middle of the switching element in Fig. 4 is the RAM area. The sixteen input circuits can be seen on the upper left hand side. The eight outputs are located below, also left of the RAM area. The block on the right-hand side is the control part, designed as full-custom part.

In this SE, all information cells are written into a common buffer from all the input lines and are transmitted via the output lines from this central buffer. In order to keep the memory access speed within the range given by technological constraints, a wide parallel memory interface is used. A central control with address queues assigned to the outputs takes care of the correct switching of the cells.

Each input port of the switching element contains a separate circuit for phase alignment and cell synchronization. Received unassigned cells are detected and discarded. Incoming cells with an error within the internal header are also detected and discarded. If there are no information

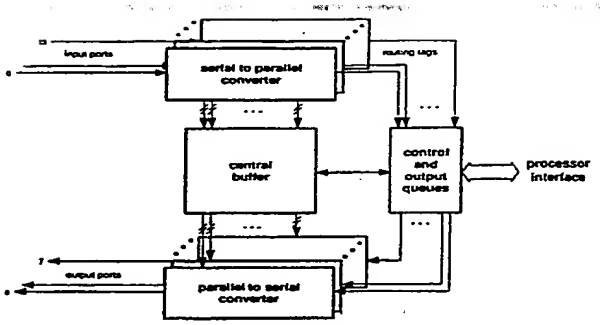

Fig. 3. ATM switching element SE 16/8.

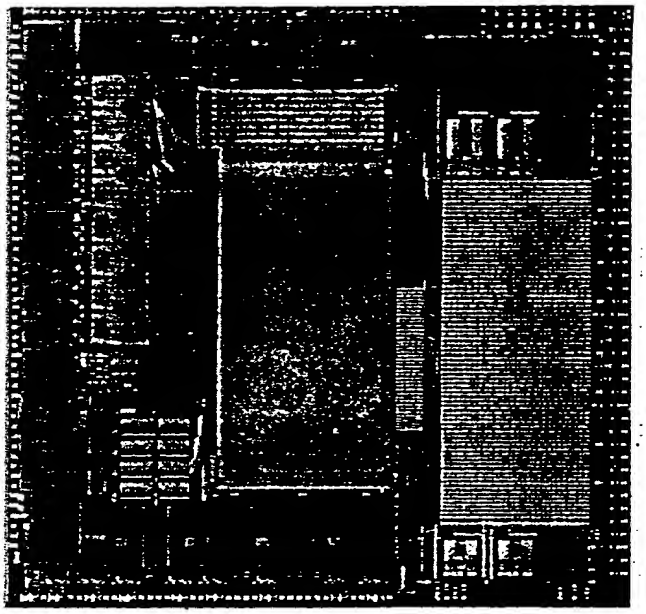

Fig. 4. Chip layout of the switching element.

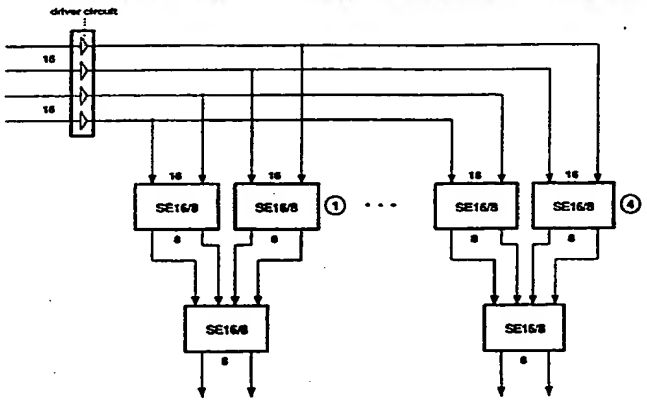

Fig. 5. ATM switching module structure.

cells for a certain output port, unassigned cells are generated.

In addition to the switching function, the switching element contains functions for its internal checking. The internal data paths are protected. A sophisticated control supervision has been implemented by a continuous monitoring of the correct operation.

The SE 16/8 (16 inputs/8 outputs) has been developed within the RACE project 1012 BLNT (broadband local network technology) [9].

2) ATM Switching Module: The ATM switching module with 32 inputs and 32 outputs (ASM 32) is implemented by a single printed circuit board representing a nonblocking, single-stage arrangement. To form this module, twelve switching elements (16 × 8) are interconnected in a funnel-like structure as shown in Fig. 5. Each funnel represents a 32 × 8 matrix, of which there are four in parallel. A single routing tag controls the path of a cell through the whole ATM switching module. Routing happens such that the switching element in the first stage of the funnel accepts a cell with the appropriate value in the self-routing header. The cell is routed through the first switching element to the defined output and switched again in the element in the second stage of the funnel arrangement. Thus, cells destined for a particular output of the second stage can only come from two inputs of the second stage. This reduces congestion in the second stage significantly.

The module is equipped with a processor, which is responsible for safeguarding and testing functions. For this purpose, it has access to all switching elements.

3) Interface Modules: The interface modules for access to the ATM switching network perform high-speed cell processing functions. They are interconnected via the switching network or a statistical ATM multiplex unit. This subsection describes the ATM-relevant part for cell processing in the above-mentioned interface modules by the example of an SLMB or TIU (see Fig. 6). The access of all these modules to the switching network is achieved using the internal cell structure, which envelopes the standardized cell format.

The interface modules contain upstream and downstream functions. Upstream functions are those which are needed for processing of ATM cells arriving in the ATM exchange. Downstream functions are needed for processing of ATM cells leaving the ATM exchange.

Upstream Direction

- *STM-1 disassembler* extracts the information data stream of the virtual container (VC-4) of the STM-1 frame. It also realizes a speed adaptation between the external and internal bit rate.
- *Cell synchronization* determines the start of the ATM cells in the continuous information bit stream. The determination is done by the header error control (HEC) mechanism.
- *Error detection and correction* of the external cell header according to the algorithm using the header error control (HEC) field as defined by CCITT.
- *Header conversion* is achieved by means of a con-

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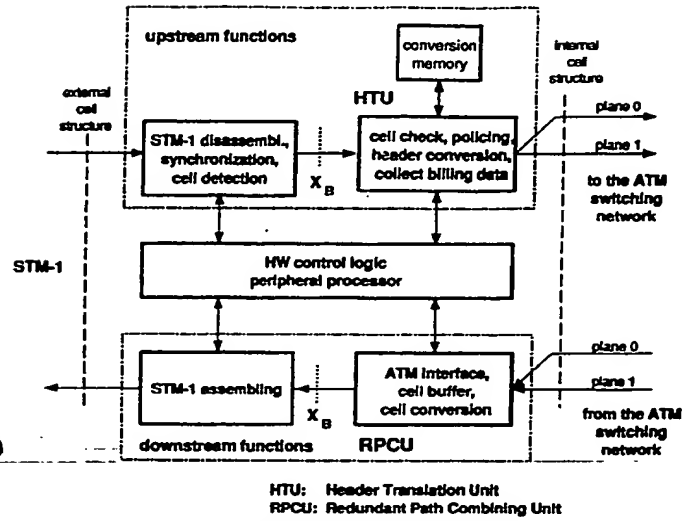

Fig. 6. Block diagram of SLMB/TIU.

version memory. This memory contains all connection individual data. Each entry is written during the call setup phase by the peripheral processor. It contains the following entries: a *flag*, which indicates whether there is an established connection for the arriving cell or not, the new *header* for the outgoing ATM cell; in particular, the new VCI and VPI values, the *information* for the switch internal additional header part of the cell (basically, this is routing information), and *cell counters* for billing functions and policing. After header conversion, the new value for the HEC field is generated and the cell is extended into the system internal cell structure.

- *Policing*. The access unit monitors every established ATM connection [10]. An ATM connection can be a virtual channel (defined by the VCI field) or a virtual path (defined by the VPI field in the cell header). For every connection and priority class, the mean and peak value of the incoming information bit rate is supervised using a leaky bucket algorithm.
- *Cell counting* for billing. For each individual connection, counters are summing up the number of cells transmitted by the subscribers. These counters are read by the control (GP) to process the billing information.

Downstream Direction

- *ATM switching network interface*, which supports the redundancy structure of the switching network (redundant path combing unit, (RPCU) described below). Only correct cells, coming from the switching network, are passed on to the exchange external transmission line.
- *Cell conversion* is needed in order to convert the exchange internal cell structure to the external structure defined by CCITT.
- *STM-1 assembler* fills the ATM cells into the VC-4 container of the STM-1 frame. Besides the SDH-related functions, clock adaptation between the internal and external clock is performed.

D. Redundancy Concept

1) Requirements for Redundancy of ATM Switches: Public switching systems have to be in service without any interruption for nearly their whole lifetime. But any element of a switch bears a specific probability to fail, and so the system must be structured such as to provide a reliable and secure service, even in a system with partly defective elements. Usually, this is achieved by using multiple parallel units and additional paths to interconnect the parallel redundant units. In case of a failure in one element, at least one alternate path must be available to avoid corruption of user data.

It has to be guaranteed that as a result of a fault (either permanent or transient),

a) user data (i.e., ATM cells) are neither duplicated nor discarded,

b) corrupted ATM cells have no impact on other existing virtual connections, and

c) that a failure of components will have no impact on the existing connections.

It is required, that existing connections are not affected by any failure in the system, and that the probability for loss or corruption of user information is negligible.
From the control point of view, the following goals have to be achieved.

- Call processing and path hunting should be done on a virtually perfect system, i.e., even failures of higher order, in practice, do not affect the correct operation.
- Failures in a component, causing a single path to fail, should be reported immediately. This must be possible under high load but also on a completely idle system without user traffic.
- Besides the supervision of the normal paths through the system, all additional paths and components used only to detect a failure and to bypass them, have to be checked for correct operation, as well.
- The normal operation of the whole system must not be influenced by housekeeping checks of the redundant units, e.g., switchover to a parallel unit must be possible under normal load without any impact on user information.
- Replacement of modules including their testing and putting them back into service has to be possible without any corruption of existing connections.

2) Basic Principles for Redundancy: Usually, switching systems operate either in load sharing or hot stand-by mode of duplicated parts. The failure units have to be small and additional paths between parallel units allow at least one operating path through the system.

- *Load sharing:* Information is routed along one of several possible paths, aiming to equally loaded parts of the system. Between failure units, a switch selects one path towards the destination. Detecting the breakdown of a failure unit, the redundancy switch preceding this fault has to be informed about the actual configuration, and all

user data have to be routed around the fault. Some time is required for this operation and existing connections will be disturbed. Therefore, load sharing is not an appropriate principle.

- *Hot stand-by:* Information is copied and switched over parallel units. After each unit, the user data from both parallel units is compared and only correct information is forwarded. This requires additional connections between the parallel units to interconnect them, and special checking modules to compare both information streams. All these additional components have to be supervised, and their correct operation (in case of an error in one switching unit) must be guaranteed.

According to the requirements for new switching systems, only hot stand-by appears to be practicable for a new ATM switching network. But to use this principle with traffic, which is characterized by statistical cell arrival processes (in an ATM switch), in the same way as for traffic characterized by deterministic arrivals of data units (STM switch) is nearly impossible. Usually, after each failure unit the information streams have to be compared. Therefore, both streams have to be identical (ATM cells in identical order), and completely synchronous (same delay for one cell in both parallel units, e.g., in two parallel switching planes). As a consequence, both parallel units (switches, multiplexers, $\cdots$) have to be operated bit synchronously and information-synchronously. This is technically nearly impossible in an ATM fabric, particularly when sporadic errors or maintenance actions (module exchange) are taken into account.

3) ATM-Based Redundancy: For the ATM switching network, a new mode of hot stand-by operation on duplicated, parallel planes has been designed. The cells are duplicated in all peripheral units connected to the switching fabric and switched over two identical, parallel planes. The paths through the parallel switching planes are identical, because all copies of a single cell have the same self-routing header. The outgoing peripheral units have interfaces to both parallel switching planes. During normal operation, each plane delivers one copy of an ATM cell, and the "redundant path combining unit (RPCU)" ensures that only the first correct copy of a cell is forwarded, whereas all other copies of the same cell are discarded within that unit. This can be achieved by internal information contained in each cell and without synchronization of the parallel switch planes.

The benefits of the new redundancy structure are as follows.

- No synchronization between parallel switching planes is required.
- The redundancy principle operates on a virtual connection basis. Outage of parts in one switching plane does not affect the traffic within the remaining parts of this plane. Even when different parts in all switching network planes fail, correct operation of the system is guaranteed as long as each VC/VP has one error-free path.
- Sporadic errors in one plane do not affect existing connections.
- The impact of a failure in a single component is limited to the virtual connections switched across this particular element. The failure unit is identical to that element, and no other connections are affected.
- The redundancy principle works without any supervision or additional functions by the control. Therefore, call processing can be done on a virtually perfect switch without restrictions.

Only two additional units are necessary for an ATM pipe: at the distribution point and at the recombination point.

- The duplication function may be combined with the header translation unit (HTU), which adds the self-routing header and converts the cell format from the external to the internal definition. Then, the cells are duplicated and switched across the parallel planes.
- The redundant path combining unit (RPCU) maintains all information required to select the correct cells of a particular virtual connection. After acceptance of a cell, the internal header is stripped off, bringing the cell back to the external format.

4) Additional Frame Check: As an additional advantage, the redundancy principle offers the possibility to cover all cells by a frame check sequence (FCS). This FCS is generated by the HTU (header translation unit) prior to cell duplication and checked at the RPCU to determine the correctness of the received cells. An erroneous cell is discarded and a copy of that cell, received from the other switch plane, must be used. Therefore, the parallel switching network will appear to be nearly error-free and only a failure of a least two switching elements on the same path in different planes will cause unrecoverable errors. Sporadic errors, e.g., within the memory, are detected by the FCS and the error-free copy of the cell is forwarded. Defects in a single element within one of the redundant planes will only have an impact on the connections switched across this particular element, and traffic carried by the remaining parts of this plane is not affected. Therefore, the overall error probability is extremely low.

E. Switching Network

1) Switching Network Structure: In order to achieve a scalable architecture, a modular approach for the switching network structure has been adopted (cf. also [11]). The network consists of multiple switching modules which can be arranged, for example, in a two-stage folded configuration with the capability for short paths in the first stage. According to Fig. 7, which shows the generic structure, and Fig. 8 showing a number of different configurations as examples, a maximum of 512 bidirectional ports can be achieved with the two-stage folded configuration using switching modules with 32 inputs and 32 outputs (32 $\times$ 32 matrix, ASM32).

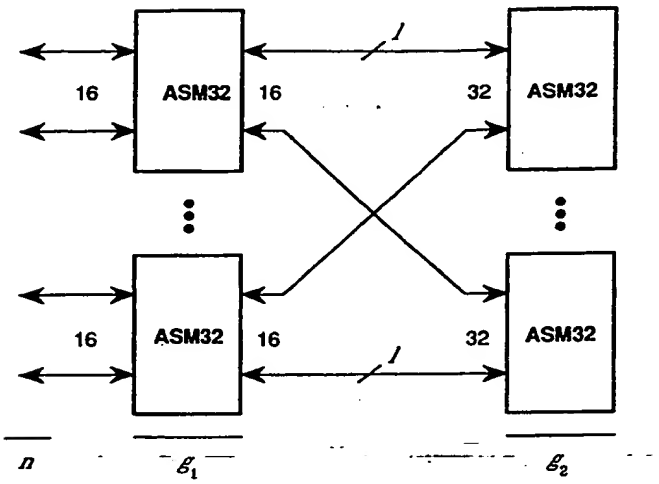

Fig. 7. Generic switching fabric structure.

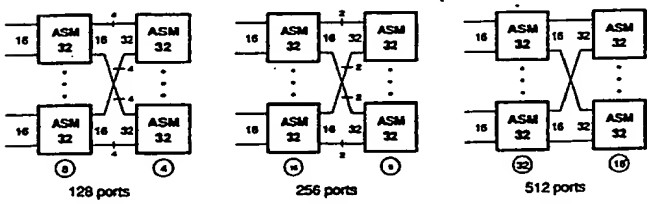

Fig. 8. Examples for switching network structures.

Using the switching elements described above, it is possible to build different types of modules, e.g., a 16 × 16 matrix, for a very economical implementation of small systems. Furthermore, using any type of module also different switching network structures can be built including straight arrangements with and without expansion to a larger number of interstage links in order to reduce blocking effects if required.

A major advantage of the chosen structure is the fact that no synchronization between modules is required, which implies that no timing problems occur. Switching modules are only supplied by a common clock from a central clock generator. Bit and cell synchronization is performed in every switching element.

The chosen structure is very flexible with respect to growth of the switching network. If only a few ports are needed, the network consists of a single switching module. For a larger number of ports, the full number of modules in the second stage for a given configuration are provided. The first stage can be partly equipped, and modules can be added up to the maximum number as the need arises. Configurations are identified by the maximum number n of ports ($n = 32\ g_2$), which can be reached with a given number, g_2 of modules in the second stage.

2) Growth Strategy: Growth of the switching network is achieved without service interruption (without loss of existing connections). This is valid for growth within a particular configuration as well as for the transition between configurations.

In most cases, the second stage of the network will be equipped with modules according to the planned maximum configuration of the switching system. Then an upgrade can be performed by adding only first-stage modules up to the maximum number for the given configuration without the need for any recabling.

In the case where the maximum number of modules in the first stage is already in service, upgrading to a new configuration means doubling the number of second-stage modules and cutting the size of the links between stages into halves.

In order to ensure an upgrade of the second stage without service interruption, two requirements have to be met.

1) During the time of reconfiguration, one plane must be able to handle the traffic without the redundant one.

2) Routing labels for existing connections must not change due to the reconfiguration.

The first requirement is met by the redundancy structure anyway. The second requirement can be met by an appropriate recabling strategy as outlined below.

The basic upgrade procedure works as follows.

- Take one plane out of service. (The redundant plane is still in operation.)
- Perform recabling and introduction of additional switching modules for the second stage.
- Test the new configuration off-line.
- Take the upgrade plane into service again.
- Do the same for the other plane.

Logically, this upgrade can be perceived as cutting the second-stage modules into halves where one module now handles the upper half of the link and the other module handles the lower half as outlined in Figs. 9 and 10, which show, as an example, the upgrade of a 128 structure into a 256 structure. The dashed lines represent those links which have to be modified. It can easily be seen that routing labels for existing connections do not change through the upgrade.

Care has to be taken that, during the upgrade operation, no connections exist such that they would be interrupted. In the example of Fig. 9, this would happen, for a connection entering the second stage through port 1 and leaving through port 7. Since, prior to the upgrade, links entering the second stage through ports $1 \cdots 4$ are logically equivalent, this restriction could only mean a slight performance degradation in terms of loss of newly arriving calls (from a traffic point-of-view, this means link separation). However, this should not be of real significance because the switching fabric has to be dimensioned such that it shows reasonable performance for single linkage also.

In any case, semipermanent connections should always be routed such that they would not be interrupted by upgrading to a single linkage structure. If advantage should be taken of the larger links in smaller structures, the path hunting algorithm should only switch connections such that they fit into the structure to be achieved by the up-

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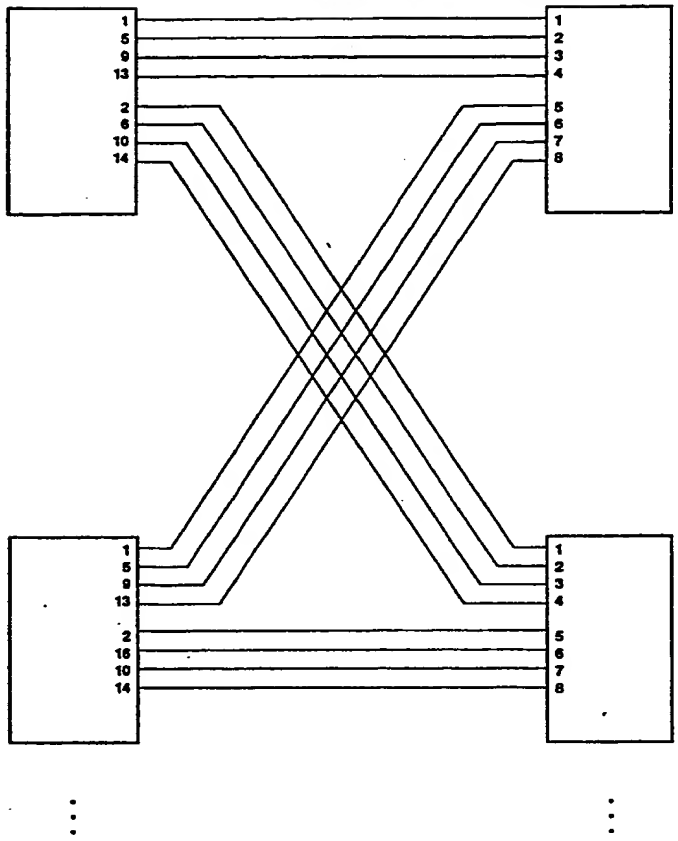

Fig. 9. Example structure before the upgrade.

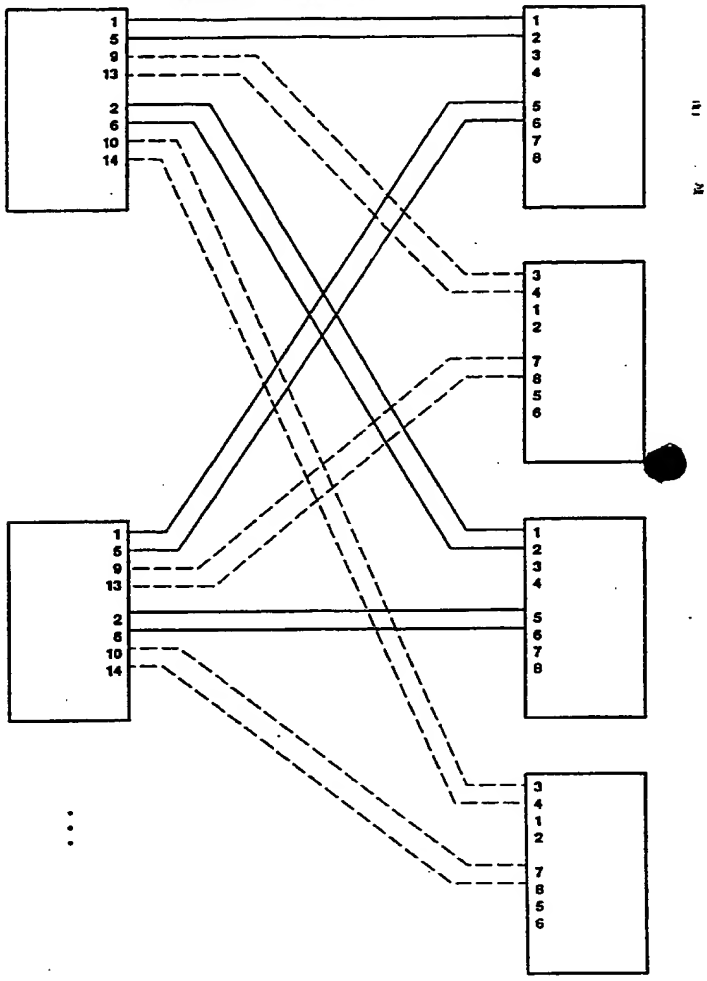

Fig. 10. Example structure after the upgrade.

grading operation, during an adequate amount of time before the actual hardware upgrade takes place. This can be done by a simple change of parameters for the path hunting algorithm during operation.

3) Performance Aspects: Performance of an ATM switching network is reflected by a number of different quantities which are mutually dependent. The major quantities of interest are call blocking probability, cell loss probability, fixed cell delay, queueing delay (cell delay variation, delay jitter). Of these quantities, the fixed cell delay is only dependent on the structural properties of the switching network. Since it is in the order of magnitude of a few cell durations, i.e., low tens of microseconds, it is only of minor importance.

By means of an approximate numerical analysis, assuming a superposition of Bernoulli arrival processes at each input, and probabilistic routing, the central buffer size has been dimensioned such as to reach a cell loss probability of less than 10^{-12} at 85% load per output of the switching element.

For this analysis, the queue length distributions of each logical output queue have been calculated by means of an exact analysis for Bernoulli arrivals. By convolving these distributions, an approximation for the buffer contents distribution of the shared buffer has been obtained. This is an approximate approach since the individual queue length distributions are not mutually independent. (The output queues are fed by a set of common inputs. A cell arriving in an output queue from a certain input cannot be part of the arrival process of another queue.)

The total queueing delay (sum of the queueing delays through both stages) of the funnel structure in the switching module has been investigated by means of detailed simulation studies. Comparison with results for a single-server queueing system with the same load characteristics has shown that there are no significant differences between the two structures in terms of queueing delay. There is only one exception: in the case of uneven load, the cell streams passing through the switching element which is less loaded experience significantly less delay compared to the other streams. From an application point of view, however, it can be claimed that the two structures are roughly equivalent in terms of queueing delay. Assuming that there is a monotonous relationship between the mean queueing delay and the cell loss probability, we can also claim that in terms of cell loss probability the funnel structure behaves roughly like the corresponding single server queue.

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For the determination of the call blocking probability, simulation studies have been carried out. The largest structure with 512 bidirectional ports (single linkage) has been used as the basis for investigations. Using smaller structures with multiple linkage leads to smaller call blocking probabilities. It was assumed that the total offered traffic consists of a mix of 2 Mb/s (5%), 10 Mb/s (20%), and 34 Mb/s (75%) calls. Assuming peak bit rate reservation as the resource allocation strategy and an admissible cell load of 85% per ATM pipe, the call blocking probability for 34 Mb/s calls is less than 10^{-3} for a carried load volume of 75 ErlMb/s per port. It has been assumed that the ports are evenly loaded. For the calls with lower bit rate, the call blocking probability is significantly lower. Furthermore, employing a more sophisticated resource allocation strategy leads to a further decrease of this quantity.

III. Conclusion and Outlook

We have presented a scalable architecture for an ATM switching system which can be enhanced from very small to very large numbers of ports with minimum initial investment.

In a further development step, the switching of bit rates in the range of 600 Mb/s and 2.4 Gb/s is envisaged. These requirements are mainly due to the application of the system as ATM cross connect.

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